		O-1449 (modified)	ATTY. DKT. NO. 5181-37601		SEF	SERIAL DIO 10/044,487		
List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)			APPLICANT: Bodo K. Parady FILING DATE: January 11, 2002		1	GROUP: 2183 6		
		Ţ	J.S. PATENT	DOCUMENTS		P. S.	CETY	
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HCO +	A1	"Load Latency Tolerance In Dynamically Scheduled Processors"; IEEE 1998; Srinivasan & Lebeck; Duke University, Department of Computer Science; Durham, North Carolina						
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1700	A3	"Understanding the Differences Between Value Prediction and Instruction Reuse"; Sodani & Sohi; University of Wisconsin-Madison, Computer Sciences Department; Madison, Wisconsin						
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DATE CONSIDERED:

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.